REMARKS

Claims 1-4 are all the claims pending in the application. Reconsideration and allowance of all the claims are respectfully requested in view of the following remarks.

Claim Rejections – 35 U.S.C. § 103

The Examiner rejected claims 1-4 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 6,193,132 to Shibata et al, (hereinafter Shibata), in view of U.S. Patent 6,337,489 to Matsumoto et al. (hereinafter Matsumoto). Applicants respectfully traverse this rejection because the references fail to establish *prima facie* obviousness for at least the following two reasons.

First, the Examiner procedurally has failed to establish *prima facie* obviousness in that he has failed to explain, with specificity, at least one of the rejections. See: *Ex parte Blanc*, 13 USPQ2d 1383 (Bd. Pat. App. & Inter. 1989); and MPEP § 2142.

Specifically, in this case, the Examiner fails to set forth how he interprets Shibata and Matsumoto so as to teach or suggest:

a chip recognition camera focused so as to recognize a lower surface of a chip when the lower surface of the chip is located substantially on a level with a chip bonding surface of a substrate, as set forth in claim 1, or

a chip recognition camera that is focused so as to recognize a lower surface of the chip when the lower surface of the chip is located within ±5 mm of a plane in which is located a chip bonding surface of a substrate, as set forth in claim 4.

That is, the Examiner makes no mention of these elements in the reasoning for his rejection. In fact, the Examiner impermissibly appears to ignore these claim elements.

Second, Shibata and Matsumoto fail to render obvious claims 1-4 because they fail to teach or suggest all the elements as set forth therein.

Claim 1 sets forth a bonding apparatus comprising a chip recognition camera disposed lower than a level of a substrate mounted surface of a substrate stage to thereby recognize the chip held by the bonding tool from a position below the chip, wherein the chip recognition

camera is focused so as to recognize a lower surface of the chip, when the lower surface of the chip is located substantially on a level with a chip bonding surface of the substrate.

In Shibata, the chip picked up by the bonding tool 12 is recognized by the first recognition camera 14, and thereafter the provisional bonding is performed based on the recognition result. Then, the reference mark of the substrate and the chip are detected by the second recognition camera 16 to seek the positional relationship between the substrate and the chip. This is a teaching operation. See column 6, line 10 to 62. Thereafter, the actual bonding is performed, and finally a shift amount of bonding is detected to thereby judge OK or NG of the bonding operation. See column 6, line 63 to column 7, line 40.

In contrast to the present invention as set forth in claim 1, in Shibata's apparatus the lower surface of the chip is not located substantially on a level with a chip bonding surface of the substrate. Further, although the chip 13 is recognized by the first recognition camera 14 in Shibata, it must judge OK or NG of the bonding due to bonding shift amount. Such judgment of the bonding inherently indicates that the bonding shift owing to the shift of the bonding axis (ball screw, guide, etc.) is necessarily caused as described in the background section of the present application. And Shibata never teaches or discloses specific solutions to solve that problem. In other words, because Shibata gets errors in positioning, it does not inherently recognize the chip when the chip is in substantially the same plane as the bonding surface of the substrate. And there is no motivation to recognize the chip when the lower surface of the chip is located substantially on a level with a chip bonding surface of the substrate as set forth in the claimed invention to eliminate the shift amount. To the extent that the Examiner is relying on measurements from Shibata's figures, such is impermissible because there is no indication that the drawings are to scale. And proportions of features in a drawing are not evidence of actual proportions when drawings are not to scale. When a reference does not disclose that the drawings are to scale and is silent as to dimensions, arguments based on measurement of the drawing features are of little value. MPEP § 2125.

Further, moving the chip within the focus range is not the same as locating the chip substantially on a level with the substrate at the recognition by the camera since a certain

physical range exists in the focus range, the lower surface of the chip is not located substantially on a level with a chip bonding surface of the substrate.

Moreover, Matsumoto teaches a chip recognition camera 8 that recognizes a bonding surface of a chip 23. However, there is no teaching or suggestion as to where the chip 23 is located relative to the substrate 22 when recognized by the camera 8.

Accordingly, even assuming that one of ordinary skill in the art were motivated to combine Shibata and Matsumoto as suggested by the Examiner, any such combination would still fail to teach or suggest a chip recognition camera disposed lower than a level of a substrate mounted surface of a substrate stage to thereby recognize the chip held by the bonding tool from a position below the chip, wherein the chip recognition camera is focused so as to recognize a lower surface of the chip, when the lower surface of the chip is located substantially on a level with a chip bonding surface of the substrate, as set forth in claim 1.

Claim 4 sets forth a bonding apparatus comprising: a bonding tool for holding a chip; a substrate stage for mounting a substrate; and a chip recognition camera disposed lower than a level of a substrate mounted surface of the substrate stage to thereby recognize the chip held by the bonding tool, wherein the chip recognition camera is focused so as to recognize a lower surface of the chip when the lower surface of the chip is located within ± 5 mm of a plane in which is located a chip bonding surface of the substrate.

For example, as shown in Figs. 1 and 2A, a chip bonding apparatus comprises: a bonding tool 2 for holding a chip 1; a substrate stage 4 for mounting a substrate 3; and a chip recognition camera 11 disposed lower than a level of a substrate mounted surface of the substrate stage 4 to thereby recognize the chip 1 held by the bonding tool 2, wherein a lower surface of the chip 1 is recognized by the chip recognition camera 11 when the lower surface of the chip 1 is located within ± 5 mm of a plane in which is located a chip bonding surface of the substrate 3.

As discussed in paragraphs 3 and 4 of the present specification, when the constituent members of a bonding tool age, the accuracy in positioning of a chip with respect to a substrate deteriorates so that there is a deviation between the position of the chip and the desired position of the chip. The deviation in position is due at least in part to the fact that in the prior art, the

chip is image recognized at a position higher than the level of the chip bonding surface of the substrate. See also Figs. 3A and 3B.

According to the arrangement of claim 4, however, because the image recognition of the chip is performed in the position where the substrate 3 and chip 1 should be bonded to each other, the substrate 3 and chip 11 can be bonded accurately without deviation.[1] That is, the deviation will not be larger than 1 μm because the error between the level of the lower surface of the chip 1 and the level of the chip bonding surface of the substrate 3 at the time of the image recognition is within ± 5 mm.[2]

In contrast to that set forth in claim 4, Shibata and Matsumoto do not teach or suggest a bonding apparatus wherein the lower surface of the chip is positioned within ± 5 mm of a plane in which is located a chip bonding surface of a substrate.

Shibata teaches that the camera 14 recognizes an image on the chip 13 when the chip is at a position significantly higher than the chip bonding surface of substrate 11. See Fig. 5, wherein the relative positions of the chip 13 and substrate 1 are shown.

Matsumoto discloses that a chip 23 is recognized by a camera 8. However, Matsumoto fails to teach or suggest a specific relationship between chip 23 and the bonding face of the substrate 22 at the time the chip 23 is recognized by the camera 8. Accordingly, Matsumoto fails to teach or suggest a chip recognition camera focused so as to recognize a lower surface of a chip when the lower surface of the chip is located within ± 5 mm of a plane in which is located a chip bonding surface of the substrate, as set forth in claim 4.

Therefore, for the sake of argument, even assuming that one of ordinary skill in the art were motivated to combine Shibata with Matsumoto as suggested by the Examiner, any such combination would still not teach or suggest a chip recognition camera focused so as to

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[1] Specification at paragraphs 21 and 24.

[2] Specification at paragraph 22.

recognize a lower surface of a chip when the lower surface of the chip is located within ± 5 mm of a plane in which is located a chip bonding surface of the substrate, as set forth in claim 4.

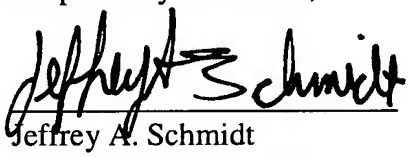
For at least any of the above reasons, Shibata and Matsumoto fail to render obvious Applicants' claims 1-4.

Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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